S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Gary R. Gilliam	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.221US5
Title:	ON-CHIP SUBSTRATE REGULATOR TEST MODE	

PRELIMINARY AMENDMENT

BOX PATENT APPLICATON
Commissioner for Patents
Washington, D.C. 20231

Sir:

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE SPECIFICATION

On page 1, line 3, before the heading "Field of the Invention," insert the following paragraph:

Cross Reference to Related Application(s)

This application is a division of U.S. Application No. 09/065,139, filed on April 23, 1998, which is a division of U.S. Application No. 08/520,818, filed on August 30, 1995, now issued as U.S. Patent No. 5,880,593, the specifications of which are hereby incorporated by reference.

Please substitute the following paragraphs of the Specification with the paragraphs in the appendix entitled "Clean Version of Specification Paragraphs." Following are marked-up versions of the amended paragraphs showing specific changes:

The paragraph beginning on page 4, line 19, is amended as follows:

For example, in Figure 1, the non-test condition of EN1 may be at a logical [los] low so that the MOSFET M3 is in the diode chain because the MOSFET M4 is off. The non-test condition of EN2 may be at a logical high so that the MOSFET M5 is essentially shorted out of the diode chain because the MOSFET M6 is on. Therefore, the voltage level of the substrate at node Vbb, under non-test conditions, is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by the three MOSFETs M1, M2 and M3. Under test conditions, the

voltage level at node Vbb can be made more positive by raising the control signal EN1 to a logical high. Such an enabling of the control signal EN1 turns on the MOSFET M4 which essentially shorts the channel of the MOSFET M3 thereby removing the MOSFET M3 from the diode chain, so that the voltage level at Vbb is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by only the MOSFETs M1 and M2. The normal substrate voltage level at Vbb can then be restored by returning the control voltage EN1 to a logical low.

The paragraph beginning on page 6, line 16, is amended as follows:

The addition of the MOSFETs M7, M8, M9 and M10 to the circuit increases the adjustability of the substrate voltage level Vbb, beyond that of the circuit shown in Figure 1. For example, the non-test condition for the control signals EN1 and EN2 may be a logical [los] <u>low</u> so that the MOSFETs M3 and M5 are in the diode chain. The non-test condition for the control signals EN3 and EN4 may be a logical high so that the MOSFETs M7 and M8 are essentially shorted out of the diode chain. Under test conditions, the substrate voltage level Vbb may be made more positive by raising the control signal EN1 to a logical high and essentially shorting the MOSFET M3 out of the diode chain. The substrate voltage level Vbb can then be made even more positive by raising the control signal EN2 to a logical high and essentially shorting the MOSFET M5 out of the diode chain, as well. The normal substrate voltage level at Vbb can then be restored by returning the control signals EN1 And EN2 to a logical low. The substrate voltage level Vbb, can be made more negative from its non-test condition by lowering the control signal EN3 to a logical low and thereby adding the MOSFET M7 to the diode chain. The substrate voltage level Vbb, can then be made even more negative by lowering the control signal EN4 to a logical low and adding the MOSFET M9 to the diode chain.

IN THE CLAIMS

Please cancel claims 1-18 after adding the following new claims:

19. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate: and

a test circuit coupled to the substrate, the test circuit comprising:

a plurality of resistive elements coupled together in series to form a chain of elements having two terminals, the first terminal coupled to a reference voltage source, and the second terminal coupled to the substrate; and

a plurality of switches, each switch coupled to a respective resistive element of the plurality of resistive elements to selectively bypass its respective resistive element.

20. (New) The integrated circuit of claim 19, wherein the plurality of resistive elements comprises diodes.

21. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate; and

a circuit for setting a substrate voltage level, the circuit comprising:

a first n-channel MOSFET having a first gate, a first drain, and a first source, wherein the first gate is coupled to the first drain and the first gate is coupled to a voltage reference level;

a second n-channel MOSFET having a second gate, a second drain, and a second source, wherein the second gate is coupled to the second drain and the second gate is coupled to the first source;

a third n-channel MOSFET having a third gate, a third drain, and a third source, wherein the third gate is coupled to the third drain and the third drain is coupled to the second source;

a fourth n-channel MOSFET having a fourth gate, a fourth drain, and a fourth source, wherein the fourth gate is coupled to be controlled by a first control

voltage and the fourth drain is coupled to the third drain, and the fourth source is coupled to the third source;

a fifth n-channel MOSFET having a fifth gate, a fifth drain, and a fifth source, wherein the fifth gate is coupled to the third gate and the fifth drain is coupled to the third source and the fifth source is coupled to the substrate; and

a sixth n-channel MOSFET having a sixth gate, a sixth drain, and a sixth source, wherein the sixth drain is coupled to the fifth drain and the sixth source is coupled to the fifth source and the sixth gate is coupled to be controlled by a second control voltage.

22. (New) The integrated circuit of claim 19, wherein the plurality of switches comprises a plurality of bypass transistors.

23. (New) The integrated circuit of claim 19 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that the one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

24. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to at least one diode in the series of diodes for electrically bypassing at least one diode.

25. (New) The integrated circuit of claim 24 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode in the series of diodes for electrically bypassing a plurality of diodes.

26. (New) The integrated circuit of claim 24 wherein at least one bypass transistor is coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

27. (New) The integrated circuit of claim 24 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

28. (New) The integrated circuit of claim 24 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

29. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises at least one bypass transistor coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

30. (New) The integrated circuit of claim 29 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

31. (New) The integrated circuit of claim 29 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

32. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level;

wherein the substrate voltage regulator circuit comprises a series of diodes coupled between a supply voltage source and the substrate; and

wherein the substrate voltage regulator circuit comprises a plurality of bypass transistors coupled to a plurality of diodes in the series of diodes for electrically bypassing the plurality of diodes.

33. (New) The integrated circuit of claim 32 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

34. (New) The integrated circuit of claim 32 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

35. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing at least one diode connected transistor,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

36. (New) The integrated circuit of claim 35 wherein the at least one bypass transistor is coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors.

37. (New) The integrated circuit of claim 35 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit such that at least one diode is unbypassed during normal operation but can be selectively bypassed during testing operations.

38. (New) The integrated circuit of claim 35 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit such that at least one diode is bypassed during normal operation but can be selectively unbypassed during testing operations.

39. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and at least one bypass transistor coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

40. (New) The integrated circuit of claim 39 wherein the substrate voltage regulator circuit includes a plurality of bypass transistors, each one of the plurality of bypass transistors coupled to at least one diode connected transistor in the series of diode connected transistors for electrically bypassing a plurality of diode connected transistors.

41. (New) The integrated circuit of claim 39 wherein the at least one bypass transistor is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

42. (New) The integrated circuit of claim 39 wherein the at least one bypass transistor is turned on during normal operation of the integrated circuit memory device such that the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.

43. (New) An integrated circuit, comprising:

an array of memory cells formed on a substrate;

a substrate voltage regulator circuit coupled to the substrate for setting a substrate voltage bias level, the substrate voltage regulator circuit comprising a series of diode connected transistors coupled between a supply voltage source and the substrate, and a plurality of bypass transistors coupled to a plurality of diode connected transistors in the series of diode connected transistors for electrically bypassing the plurality of diode connected transistors,

each diode connected transistor of the series of diode connected transistors has a junction voltage drop, and the substrate voltage bias level is defined by a supply voltage level minus junction voltage drops of unbypassed diode connected transistors of the series of diode connected transistors.

44. (New) The integrated circuit of claim 43 wherein the plurality of bypass transistors is turned off during normal operation of the integrated circuit memory device such that the one diode connected transistor is unbypassed during normal operation but can be selectively bypassed during testing operations.

45. (New) The integrated circuit of claim 43 wherein the plurality of bypass transistors is turned on during normal operation of the integrated circuit memory device such that the one diode connected transistor is bypassed during normal operation but can be selectively unbypassed during testing operations.

REMARKS

Claims 1 - 18 have been canceled and new claims 19 - 45 have been added. Claims 19 - 45 are now pending in this application.

The specification is amended to add a cross reference to the prior application and to correct minor typographical errors. No new matter is added by way of these amendments.

The application filing fee as calculated on the application transmittal sheet reflects the amendments to the claims described above.

The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application.

Respectfully submitted,

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Date of Deposit: August 22, 2001
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

Docket No. 00303.221US5 Micron Ref. No. 94-0108.04
WD #

Clean Version of the Amended Specification Paragraphs

ON-CHIP SUBSTRATE REGULATOR TEST MODE
Applicant: Gary R. Gilliam
Serial No.: Unknown

Please replace the paragraph beginning on page 4, line 19, with the following:

For example, in Figure 1, the non-test condition of EN1 may be at a logical low so that the MOSFET M3 is in the diode chain because the MOSFET M4 is off. The non-test condition of EN2 may be at a logical high so that the MOSFET M5 is essentially shorted out of the diode chain because the MOSFET M6 is on. Therefore, the voltage level of the substrate at node Vbb, under non-test conditions, is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by the three MOSFETs M1, M2 and M3. Under test conditions, the voltage level at node Vbb can be made more positive by raising the control signal EN1 to a logical high. Such an enabling of the control signal EN1 turns on the MOSFET M4 which essentially shorts the channel of the MOSFET M3 thereby removing the MOSFET M3 from the diode chain, so that the voltage level at Vbb is substantially equivalent to the supply voltage level Vcc, less the voltage dropped by only the MOSFETs M1 and M2. The normal substrate voltage level at Vbb can then be restored by returning the control voltage EN1 to a logical low.

Please replace the paragraph beginning on page 6, line 16, with the following:

The addition of the MOSFETs M7, M8, M9 and M10 to the circuit increases the adjustability of the substrate voltage level Vbb, beyond that of the circuit shown in Figure 1. For example, the non-test condition for the control signals EN1 and EN2 may be a logical low so that the MOSFETs M3 and M5 are in the diode chain. The non-test condition for the control signals EN3 and EN4 may be a logical high so that the MOSFETs M7 and M8 are essentially shorted out of the diode chain. Under test conditions, the substrate voltage level Vbb may be made more positive by raising the control signal EN1 to a logical high and essentially shorting the MOSFET M3 out of the diode chain. The substrate voltage level Vbb can then be made even more positive

by raising the control signal EN2 to a logical high and essentially shorting the MOSFET M5 out of the diode chain, as well. The normal substrate voltage level at Vbb can then be restored by returning the control signals EN1 And EN2 to a logical low. The substrate voltage level Vbb, can be made more negative from its non-test condition by lowering the control signal EN3 to a logical low and thereby adding the MOSFET M7 to the diode chain. The substrate voltage level Vbb, can then be made even more negative by lowering the control signal EN4 to a logical low and adding the MOSFET M9 to the diode chain.